

$$C = A \text{ or } B$$

$$A = L_3 \text{ and } C$$

$$B = L_1 \text{ and } L_2$$

Fig. 1 (Prior Art)

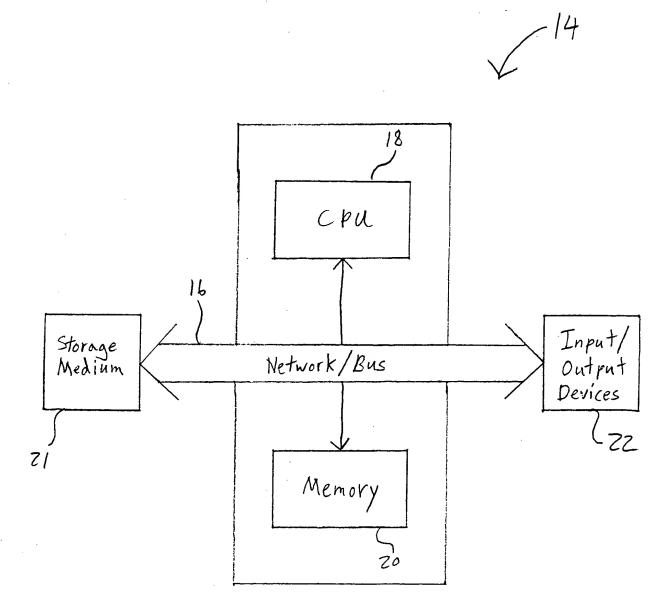


Fig. 2

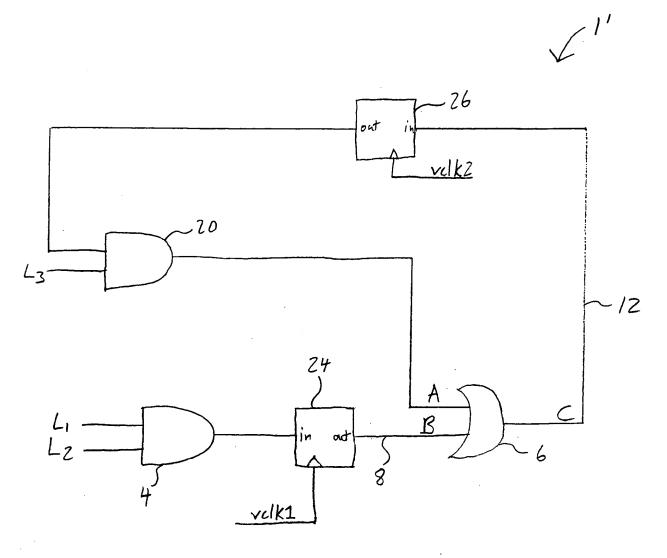


Fig. 3A

```
in_{24} = L_1 and L_2

out_{24} = if (vclk1 == HIGH) then in_{24}//change state

else out_{24}//retain state

B = out_{24}
C = A or B
in_{26} = C
out_{26} = if (vclk2 == high) then in_{26}//change state

else out_{26}//retain state

A = L_3 and out_{26}
```

```
module fig1 (L1, L2, L3, vclk1, vclk2, .. )
input L1, L2, L3, vclk1, vclk2;
       and
              g14 (in24, L1, L2);
       vdelement g24 (out24, vclk1, in24);
              g16 (in26, A, out24);
       vdelement g26 (out26, vclk2, in26);
                                                                                  -78
              g20 (A, L3, out26);
       and
endmodule
primitive vdelement (out, vclk, in)
output out;
reg out;
input velk, in;
table
// vclk data out
                     out new
 1
       1:
              ?
                     : 1;
 1
       0:
                     :0;
 0
       ?:
                     : -; // - means 'no change', i.e. retain previous value
endtable
endprimitive
```

Fig. 3B

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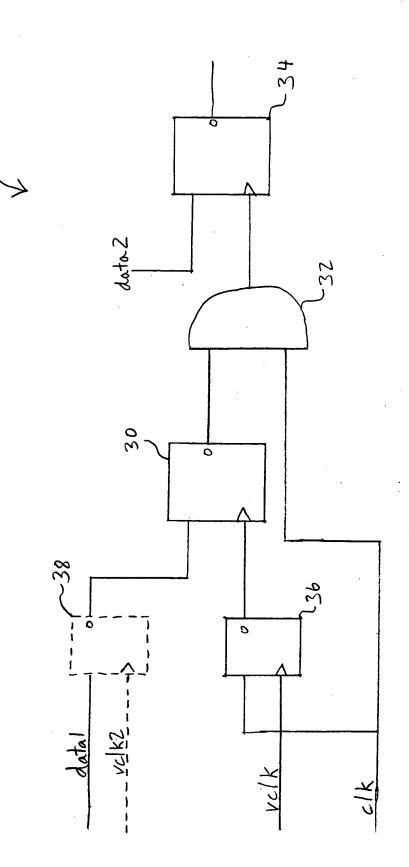


Fig. 4

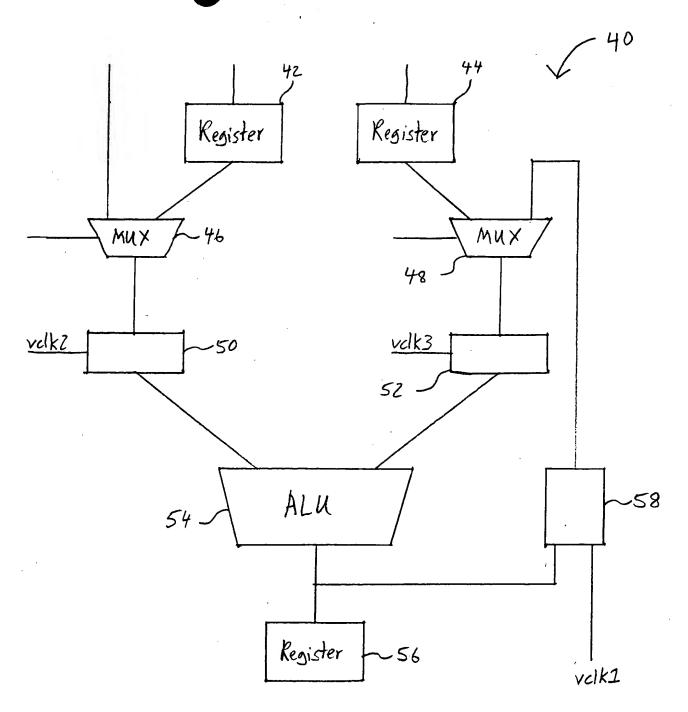


Fig. 5

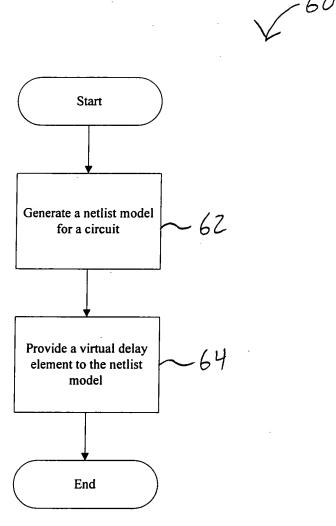


Figure 6